

METHOD OF MAKING A POWER MOSFET

Related Applications

5 This application is a continuation-in-part of U.S. Patent Appln. Serial No. 09/586,407 entitled "High Voltage Power MOSFET Having Low On-Resistance," filed on June 2, 2000.

Field of the Invention

10 The present invention relates generally to the fabrication of semiconductor devices, and more particularly to high voltage semiconductor devices such as high power MOSFET devices.

Background of the Invention

15 High voltage power MOSFET devices are employed in applications such as automobile ignition systems, power supplies, motor drives, ballasts, and power management applications. Such devices should sustain high voltage in the off-state and have a low voltage drop with high current flow in the on-state.

 FIG. 1 illustrates a typical structure for an N-channel power MOSFET. An N-epitaxial silicon layer 1 formed over an N⁺ silicon substrate 2 contains p-body regions 5 and 6, and N⁺ source regions 7 and 8 for two MOSFET cells in the device. P-body regions 5 and 6 may include shallow regions 5a and 6a as well as deep p-body regions 5b and 6b. A source-body electrode 12 extends across certain surface portions of epitaxial layer 1 to contact the source and body regions. The N-type drain for both cells is formed by the portion of N-epitaxial layer 1 extending to the upper semiconductor surface in FIG. 1. A drain electrode (not separately shown) is provided at the bottom of N⁺ substrate 2. An insulated gate electrode 18 comprising oxide and a gate conductor of polysilicon layers lies over the channel and drain portions on the upper semiconductor surface.

25 The on-resistance of the conventional MOSFET shown in FIG. 1 is determined largely by the drift zone resistance in epitaxial layer 1. The drift zone

resistance is in turn determined by the doping and the layer thickness of epitaxial layer 1. However, to increase the breakdown voltage of the device, the doping concentration of epitaxial layer 1 must be reduced while the layer thickness is increased. Curve 20 in FIG. 2 shows the on-resistance multiplied by the device area (often referred to as the specific on-resistance) as a function of the breakdown voltage for a conventional MOSFET. Unfortunately, as curve 20 shows, the specific on-resistance of the device increases rapidly as its breakdown voltage increases. This rapid increase in specific on-resistance presents a problem when the MOSFET is to be operated at higher voltages, particularly at voltages greater than a few hundred volts.

FIG. 3 shows a MOSFET that is designed to operate at higher voltages with a reduced on-resistance. This MOSFET is disclosed in paper No. 26.2 in the Proceedings of the IEDM, 1998, p. 683. This MOSFET is similar to the conventional MOSFET shown in FIG. 2 except that it includes p-type doped regions 40 and 42 which extend from beneath the body regions 5 and 6 into to the drift region of the device. The p-type doped regions 40 and 42 cause the reverse voltage to be built up not only in the vertical direction, as in a conventional MOSFET, but in the horizontal direction as well. As a result, this device can achieve the same reverse voltage as in the conventional device with a reduced layer thickness of epitaxial layer 1 and with increased doping concentration in the drift zone. Curve 25 in FIG. 2 shows the specific on-resistance per unit area as a function of the breakdown voltage of the MOSFET shown in FIG 3. Clearly, at higher operating voltages, the on-resistance of this device is substantially reduced relative to that of the device shown in FIG. 1, essentially increasing linearly with the breakdown voltage.

The structure shown in FIG. 3 can be fabricated with a process sequence that includes multiple epitaxial deposition steps, each followed by the introduction of the appropriate dopant. Unfortunately, epitaxial deposition steps are expensive to perform and thus this structure is expensive to manufacture.

Accordingly, it would be desirable to provide a method of fabricating the MOSFET structure shown in FIG. 3 that requires a minimum number of deposition steps so that it can be produced less expensively.

5 **Summary of the Invention**

 In accordance with the present invention, a high voltage MOSFET is provided that includes a substrate of a first conductivity type. An epitaxial layer also of the first conductivity type is deposited on the substrate. First and second body regions are located in the epitaxial layer and define a drift region between
10 them. The body regions have a second conductivity type. First and second source regions of the first conductivity type are respectively located in the first and second body regions. A plurality of trenches are located below the body regions in the drift region of the epitaxial layer. The trenches, which extend toward the substrate from the first and second body regions, are filled with a material that includes a dopant of
15 the second conductivity type. The dopant is diffused from the trenches into portions of the epitaxial layer adjacent the trenches, thus forming the p-type doped regions that cause the reverse voltage to be built up in the horizontal direction as well as the vertical direction. Next, the breakdown voltage in the epitaxial layer is measured and compared to a predetermined relationship between breakdown voltage and
20 diffusion time to determine a remaining diffusion time needed to achieve a prescribed breakdown voltage. An additional diffusion step is performed for the remaining diffusion time so that the resulting device has the prescribed breakdown voltage.

 In accordance with one aspect of the invention, the material filling the
25 trench is polysilicon.

 In accordance with yet another aspect of the invention, the polysilicon filling the trench is at least partially oxidized. Alternatively the polysilicon may be subsequently recrystallized to form single crystal silicon.

 In accordance with another aspect of the invention, the material filling the
30 trench is a dielectric such as silicon dioxide, for example.

In accordance with another aspect of the invention, the material filling the trench may include both polysilicon and a dielectric.

In accordance with another aspect of the invention, the trench may include both epitaxial silicon and a dielectric.

5 In accordance with another aspect of the invention, a method is provided for forming a high voltage MOSFET. The method begins by providing a substrate of a first conductivity type and depositing an epitaxial layer on the substrate. The epitaxial layer has a first conductivity type. First and second body regions are formed in the epitaxial layer to define a drift region therebetween. The body regions
10 have a second conductivity type. First and second source regions of the first conductivity type are formed in the first and second body regions, respectively. A plurality of trenches are formed in the drift region of the epitaxial layer. The trenches are filled with a material having a dopant of the second conductivity type. The trenches extend toward the substrate from the first and second body regions. At
15 least a portion of the dopant is diffused from the trenches into portions of the epitaxial layer adjacent the trenches. Next, the breakdown voltage in the epitaxial layer is measured and compared to a predetermined relationship between breakdown voltage and diffusion time to determine a remaining diffusion time needed to achieve a prescribed breakdown voltage. An additional diffusion step is
20 performed for the remaining diffusion time so that the resulting device has the prescribed breakdown voltage.

Brief Description of the Drawings

FIG. 1 shows a cross-sectional view of a conventional high voltage
25 MOSFET structure.

FIG. 2 shows the on-resistance per unit area as a function of the breakdown voltage for a conventional high voltage MOSFET and a MOSFET constructed in accordance with the present invention.

FIG. 3 shows a MOSFET structure designed to operate with a lower on-
30 resistance per unit area at the same voltage than the structure depicted in FIG. 1.

FIGs. 4-6 show the pertinent portions of various embodiments of the power MOSFET constructed in accordance with the present invention.

FIG. 7 shows a complete high voltage MOSFET constructed in accordance with the present invention.

5 FIG. 8 shows a test structure that may be used to simultaneously optimize the breakdown voltage and the on-resistance of the high voltage MOSFET shown in FIG. 7.

FIG. 9 is a graph showing an exemplary relationship between diffusion time and the breakdown voltage for the test structure shown in FIG. 8.

10 FIG. 10 is a graph showing an exemplary relationship between diffusion time and on-resistance for the test structures of FIG. 8.

Detailed Description

15 In accordance with the present invention, the p-type regions 40 and 42 shown in FIG. 3 are formed by first etching a pair of trenches that are centered about the position where the p-type regions 40 and 42 are to be located. The trenches are subsequently filled with a dopant rich material. The dopant in the material is diffused out of the trenches and into the adjacent epitaxial layer that forms the drift region of the device. The resulting doped portions of the epitaxial
20 layer form the p-type regions. The material filling the trenches, along with the dopant that has not been diffused out of the trenches, remain in the final device. Accordingly, the material should be selected so that it does not adversely affect the characteristics of the device. Exemplary materials that may be used for the material filling the trenches include polysilicon or a dielectric such as silicon dioxide.

25 FIGs. 4-6 show several different combinations of materials that may be used to fill trenches 44 and 46 that are formed in epitaxial silicon layer 1. While FIGs. 4-6 show the trenches 44 and 46, epitaxial layer 1, and substrate 2, for purposes of clarity FIGs. 4-6 do not show the upper portion of the power MOSFET structure that includes the P-body regions and the sources.

30 In FIG. 4, the trenches 44 and 46 are filled with a doped dielectric such as boron-doped silicon dioxide. After the trenches are filled, the boron is diffused into

the adjacent epitaxial layer 1 to form the p-type regions 40 and 42. The boron-doped silicon dioxide that fills the trench remains in the final MOSFET device.

In FIG. 5, the trenches are at least partially filled with polycrystalline silicon, i.e., polysilicon, that is doped with boron. After the trenches are filled, the boron is diffused into the adjacent epitaxial layer 1 to form the p-type regions 40 and 42. The remaining boron-doped polysilicon that fills the trench remains in the final MOSFET device. Alternatively, the polysilicon may be all or partially oxidized after the diffusion step is performed to form silicon dioxide. Accordingly, the trench remaining in the final MOSFET device is filled with a dielectric, i.e., silicon dioxide, and any residual polysilicon. In another alternative, any boron-doped polysilicon in the trench is recrystallized at an elevated temperature to form single crystal silicon. In this case the trench remaining in the final MOSFET device is filled with single crystal silicon, or single crystal silicon in combination with silicon dioxide or another dielectric.

In FIG. 6, the trenches 44 and 46 are first partially filled with doped polysilicon followed by the deposition of a dielectric to completely fill the trench. After the trenches are filled, the boron is diffused into the adjacent epitaxial layer 1 to form the p-type regions 40 and 42. The remaining boron-doped polysilicon and the dielectric filling the trench remains in the final MOSFET device. In some cases the boron-doped polysilicon is recrystallized at an elevated temperature to form single crystal silicon. Accordingly, the trench remaining in the final MOSFET device is filled with both single crystal silicon and a dielectric.

FIG. 7 shows the resulting power MOSFET constructed in accordance with the present invention. The MOSFET includes substrate 2, epitaxial layer 1, p-body regions 5 and 6, shallow p-body regions 5a and 6a, deep p-body regions 5b and 6b, source regions 7 and 8, and p-type regions 40 and 42 in which trenches 44 and 46 are respectively located. Also shown are the gate electrode, which includes oxide layer 48 and polysilicon layer 49, and the source-body electrode, which includes metallization layer 50.

The inventive power MOSFET shown in FIG 7 may be fabricated in accordance with any conventional processing technique. For example, the following

series of exemplary steps may be performed to form the power MOSFET depicted in FIG. 7.

An N- doped epitaxial layer 1 is grown on a conventionally N+ doped substrate 2. Epitaxial layer 1 is typically 15-50 microns in thickness for a 400-800 V device with a resistivity of 15-60 ohm-cm. Next, an oxide masking layer such as a sandwich of oxide and nitride is formed by covering the surface of epitaxial layer 1 with an oxide layer, which is then conventionally exposed and patterned to leave mask portions that define the location of the trenches 44 and 46. The trenches are dry etched through the mask openings by reactive ion etching to a depth that typically ranges from 10-40 microns. A layer of silicon (typically about 500 – 1000 Å) may be removed from the trench sidewalls to eliminate damage caused by the reactive ion etching process. First, a sacrificial silicon dioxide layer is grown on the surfaces of trenches 44 and 46. The sacrificial layer and the mask portions are removed either by a buffered oxide etch or an HF etch so that the resulting trench sidewalls are as smooth as possible.

The trenches 44 and 46 are filled with any of the previously mentioned materials such as single crystal silicon, polysilicon, silicon dioxide, or a combination thereof. During deposition, the single crystal silicon, polysilicon or oxide are typically doped with a dopant such as boron. A subsequent diffusion step is performed to diffuse the dopant out the trenches and into the surrounding epitaxial layer. If the material remaining in the trenches is single crystal silicon or polysilicon, it may be oxidized or recrystallized.

The substrate with the epitaxial layer containing the filled trenches is now ready for the conventional steps in the fabrication of a high voltage MOSFET. Gate oxide is next grown and a layer of polycrystalline silicon is deposited, doped, and oxidized. If employed, deep p-body regions 5b and 6b are formed using conventional masking, ion implantation and diffusion processes. The dose for the deep p-body regions will typically range from about 1×10^{14} – $5 \times 10^{15}/\text{cm}^2$. Next, shallow p-body regions 5a and 6a are formed using conventional implantation and diffusion steps. The p-body regions are boron implanted at 40 to 60 KeV with a dosage from about 1×10^{13} to $5 \times 10^{14}/\text{cm}^2$.

Next, a photoresist masking process is used to form a patterned masking layer that defines source regions 7 and 8. Source regions 7 and 8 are then formed by an implantation and diffusion process. For example, the source regions may be implanted with arsenic at 80 KeV to a concentration that is typically in the range of 2×10^{15} to $1.2 \times 10^{16}/\text{cm}^2$. After implantation, the arsenic is diffused to a depth of approximately 0.5 to 2.0 microns. The depth of the deep p-body region typically ranges from about 2.5 to 5 microns while the body region ranges from about 1 to 3 microns in depth. Finally, the masking layer is removed in a conventional manner to form the structure depicted in FIG. 7.

10 The DMOS transistor is completed in a conventional manner by forming and patterning the oxide layer to provide contact openings. A metallization layer 50 is also deposited and masked to contact the source-body regions and the gate conductor. A layer of passivation may next be deposited, masked and etched to define pad contacts. Finally, a drain contact layer (not shown) is formed on the
15 bottom surface of the substrate.

It should be noted that while in the previously described process the trenches are formed prior to the formation of the p-body and deep p-body regions, the present invention more generally encompasses processes in which the trenches are formed prior to, or subsequent to, any or all of the remaining doped regions. In
20 addition, while a specific process sequence for fabricating the power MOSFET is disclosed, other process sequences may be used while remaining within the scope of this invention.

The power MOSFET device constructed in accordance with the present invention offers a number of advantages over the prior art device constructed by
25 conventional techniques. For example, the vertical dopant gradient of the p-type regions is very nearly zero. The horizontal dopant gradient may be accurately controlled by varying the amount of dopant that is introduced and the number and duration of thermal cycles used in the diffusion step. Furthermore, the amount of dopant introduced and the lateral dopant gradient can be varied to optimize both the
30 breakdown voltage and the on-resistance of the device.

In the embodiment of the invention shown in FIG. 7 the p-type trench is formed below the body region. However, not every p-type trench need have a body region associated with it, particularly at the perimeter of the die or in regions containing pads or interconnections.

5 The breakdown voltage of the inventive MOSFET structure depends on the dopant concentration in the p-type regions 40 and 42. Accordingly, the more precisely the dopant concentration can be controlled, the more precisely a device having a given breakdown voltage can be achieved. The dopant concentration will be determined by the amount of dopant in the layer in contact with the surfaces of
10 the trench and the amount of time that the diffusion process is allowed to proceed.

A test structure used to simultaneously optimize the on-resistance of the high voltage MOSFET is shown in FIG. 8. The test structures include contact regions 50 and 52 at which p-type regions 40 and 42 are exposed. As used herein, the term "optimization" means that the breakdown voltage of the MOSFET is above
15 a specified breakdown voltage by an amount that provides sufficient margin, but not so much that the on-resistance of the device increases.

FIG. 9 is a graph showing the relationship between diffusion time and the breakdown voltage for the inventive test structures. This relationship will be applicable to MOSFETS having a given structure and composition which are
20 fabricated by substantially the same manufacturing process. That is, the relationship between diffusion time and breakdown voltage will be different for MOSFETS with different structures or compositions, or with substantially identical structures and compositions but which are fabricated by different fabrication techniques.

25 The relationship between diffusion time and breakdown voltage depicted in FIG. 9 can be experimentally determined. First, a series of substantially identical MOSFET structures are fabricated in which the dopant is diffused from the trenches into the adjacent epitaxial layer for different amounts of time for the range of dopant amounts found in the layer in contact with the trench surface. Next, a
30 portion of the surface layers of the device are removed to expose adjacent p-type regions 40 and 42 to form contact regions 50 and 52 (see FIG. 8.). An electrode is

placed in contact with each of the p-type regions 40 and 42 and a voltage applied to allow full depletion of the dopant so that the breakdown voltage can be measured. In this way a single data point along the curve in FIG. 9 is obtained. By repeating this procedure for the series of MOSFETs the complete curve can be generated.

5 Once this graph has been obtained, subsequent structures can be fabricated by allowing the diffusion step to proceed for a length of time significantly less than that needed to achieve the desired breakdown voltage. Typically, of course, the desired breakdown voltage will be its maximum value. The breakdown voltage of one or more of such structures is then measured in the manner described above. The
10 measured breakdown voltage is located on the graph of FIG. 9 and the differential diffusion time between the measured breakdown voltage and the desired breakdown voltage is determined. The remaining subsequent structures can then undergo an additional diffusion step for a period of time equal to the differential diffusion time. In this way the completed structures will have a breakdown voltage very nearly
15 equal to the desired maximum value.

 The relationship between the on-resistance of a high voltage MOSFET and a diffusion time is shown in FIG. 10. As this figure shows, the MOSFET should be rediffused for a sufficiently long time to obtain the desired breakdown voltage, but not so long that the device on-resistance begins to increase significantly.

20 Although various embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and are within the purview of the appended claims without departing from the spirit and intended scope of the invention. For example, a test structure for a high voltage MOSFET in accordance
25 with the present invention may be provided in which the conductivities of the various semiconductor regions of the test structure and the MOSFET are reversed from those described herein.

WHAT IS CLAIMED IS:

1. A method of forming a high voltage MOSFET comprising the steps
of:
 - 5 providing a substrate of a first conductivity type;
depositing an epitaxial layer on the substrate, said epitaxial layer
having a first conductivity type;
forming first and second body regions in the epitaxial layer to define
a drift region therebetween, said body regions having a second conductivity
10 type; .
forming first and second source regions of the first conductivity type
in the first and second body regions, respectively; and
forming a plurality of trenches in said drift region of the epitaxial
layer;
15 filling said trenches with a material having a dopant of the second
conductivity type, said trenches extending toward the substrate from the first
and second body regions;
diffusing at least a portion of said dopant from said trenches into
portions of the epitaxial layer adjacent the trenches;
20 measuring a breakdown voltage in said epitaxial layer;
comparing the measured breakdown voltage to a predetermined
relationship between breakdown voltage and diffusion time to determine a
remaining diffusion time to achieve a prescribed breakdown voltage; and
performing an additional diffusion step for said remaining diffusion
25 time.
2. The method of claim 1 wherein said material filling the trench is
single crystal silicon or polysilicon.
- 30 3. The method of claim 1 wherein said material filling the trench is a
dielectric.

5

4. The method of claim 3 wherein said dielectric is silicon dioxide.

5. The method of claim 1 wherein said dopant is boron.

5

6. The method of claim 2 further comprising the step of at least partially oxidizing said single crystal silicon or polysilicon

7. The method of claim 2 further comprising the step of recrystallizing said polysilicon to form single crystal silicon.

10

8. The method of claim 1 wherein said material filling the trench includes single crystal silicon and a dielectric or polysilicon and a dielectric.

9. The method of claim 1 wherein said body regions include deep body regions.

15

10. The method of claim 1, wherein said trench is formed by providing a masking layer defining at least one trench, and etching the trench defined by the masking layer.

20

11. The method of claim 1, wherein said body region is formed by implanting and diffusing a dopant into the substrate.

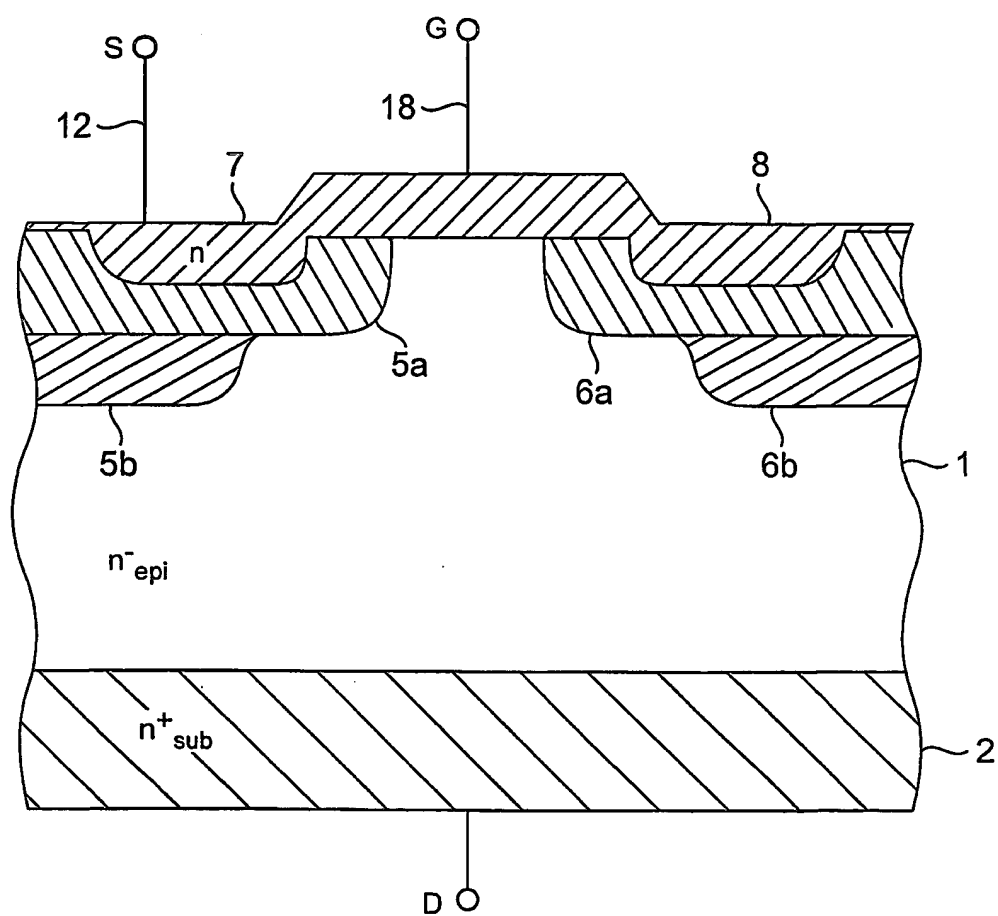
12. A high voltage MOSFET made in accordance with the method of claim 10.

25

13. The method of claim 6 further comprising the step of recrystallizing said polysilicon to form single crystal silicon.

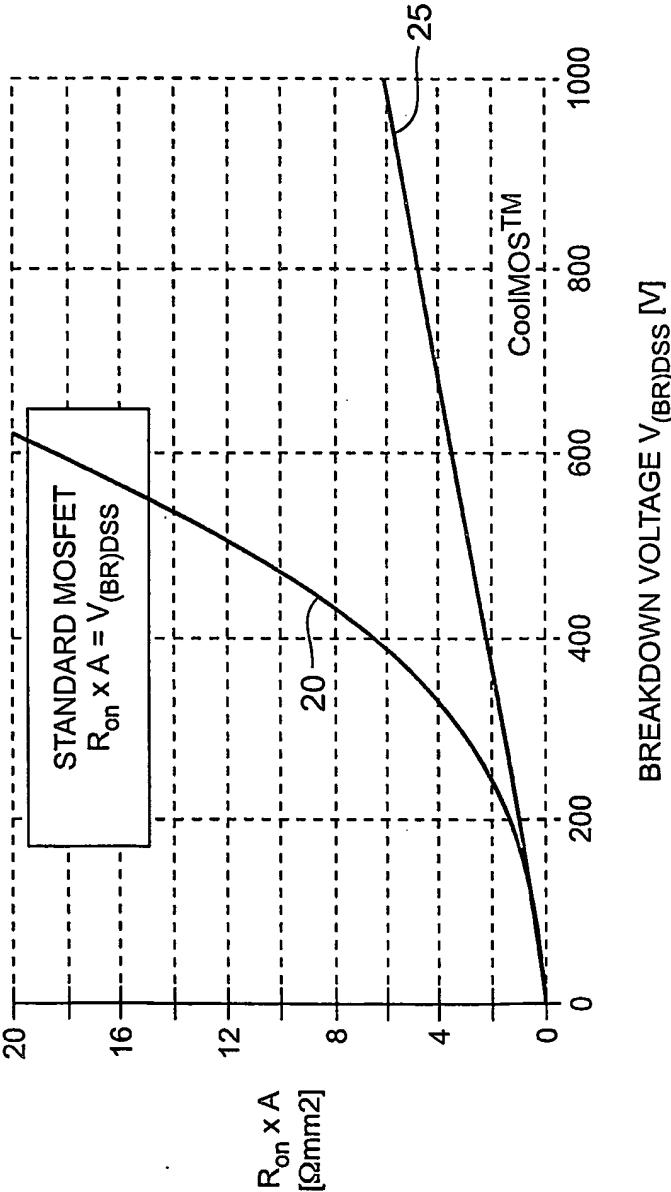
30

14. The method of claim 1 wherein said prescribed breakdown voltage is a maximum breakdown voltage.



CONVENTIONAL MOSFET

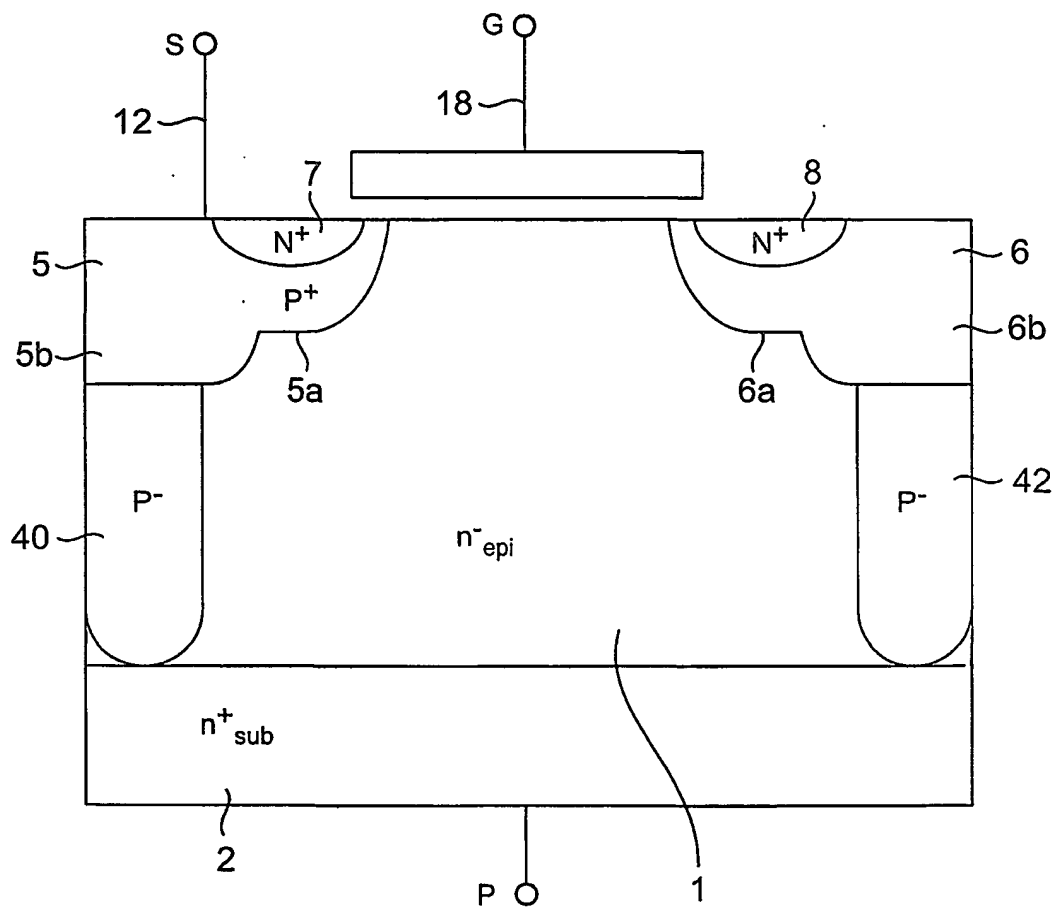
FIG. 1



THE SPECIFIC ON-RESISTANCE OF A VERTICAL DMOS TRANSISTOR WITH THE DOPANT DISTRIBUTION OF FIG. 1

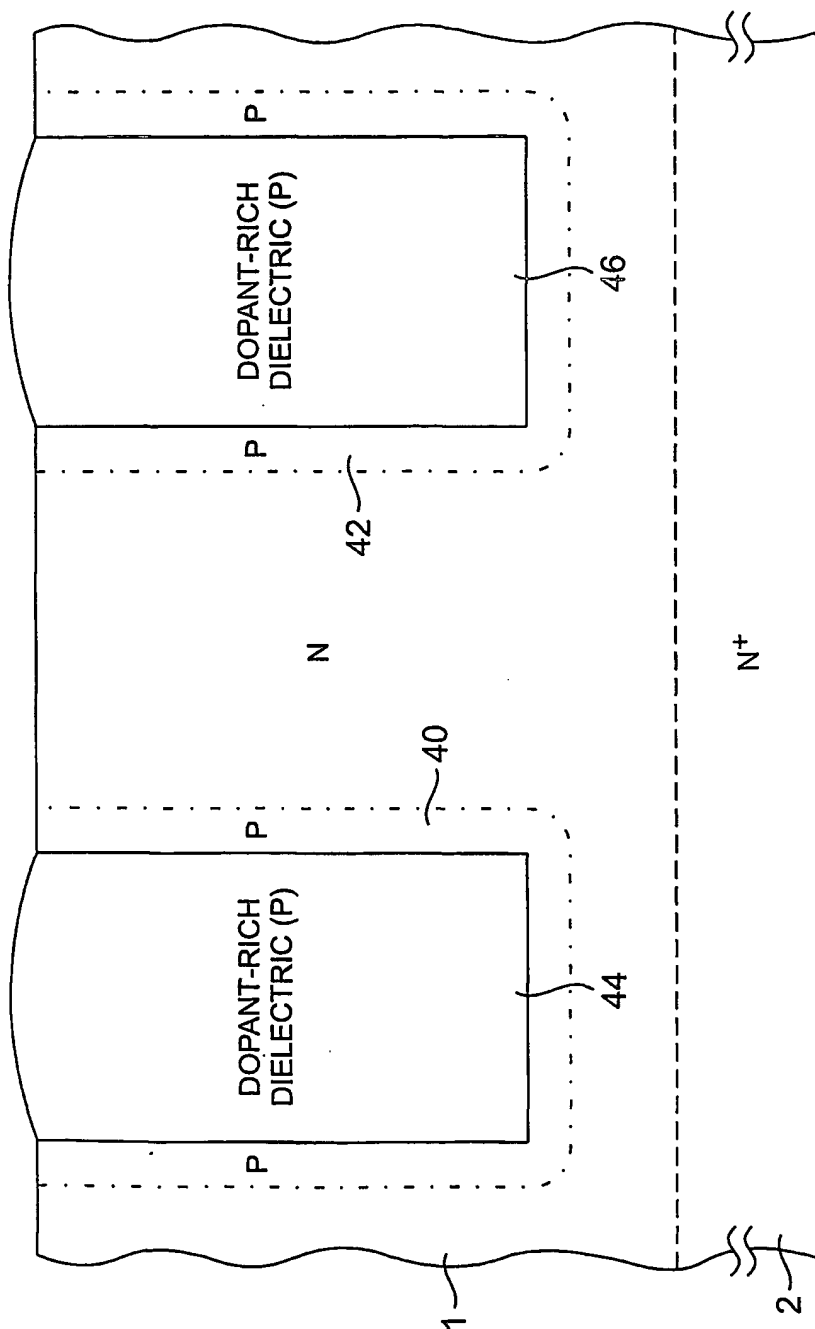
FIG. 2

3/10



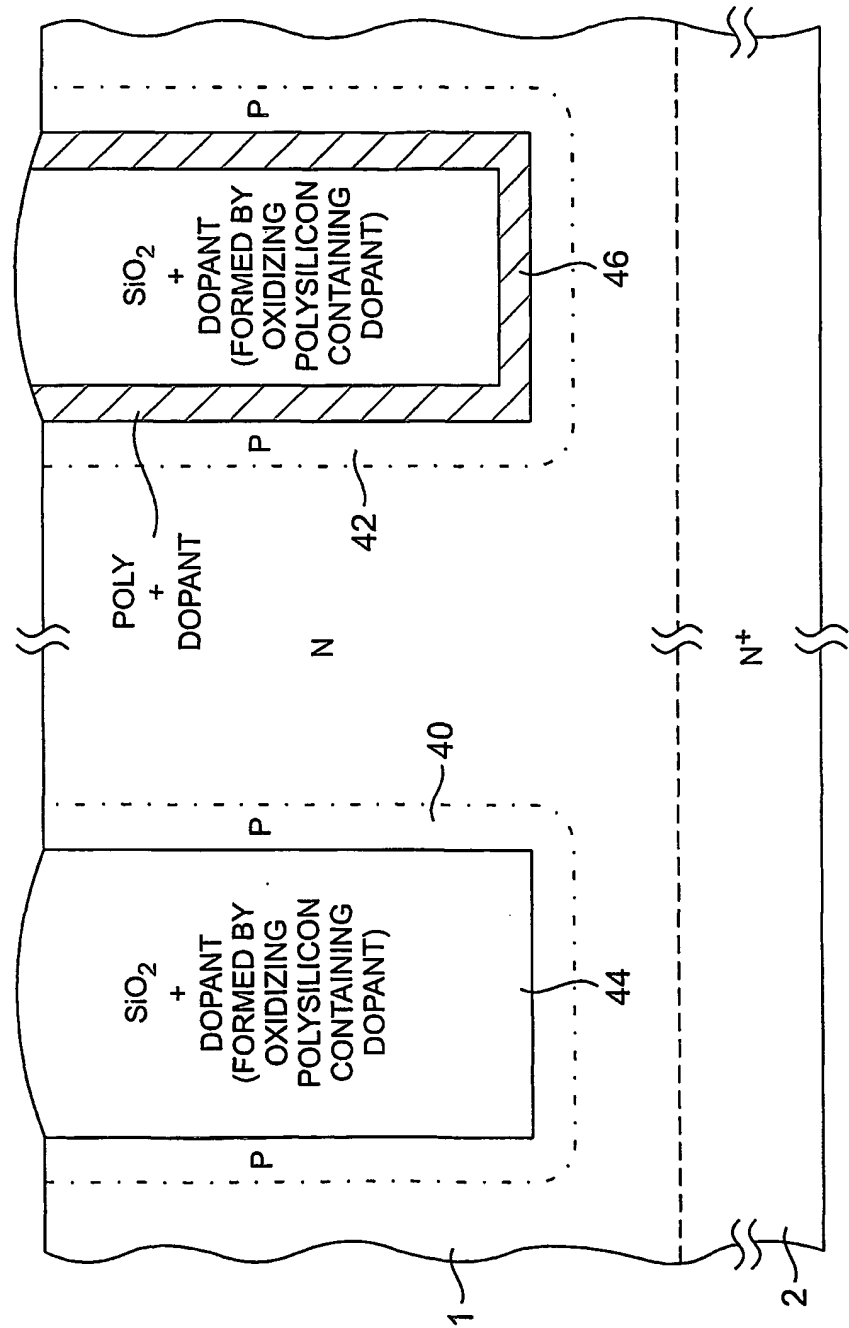
THE DOPANT DISTRIBUTION OF A
HIGH VOLTAGE VERTICAL DMOS TRANSISTOR
WITH A RELATIVELY LOW ON-RESISTANCE

FIG. 3



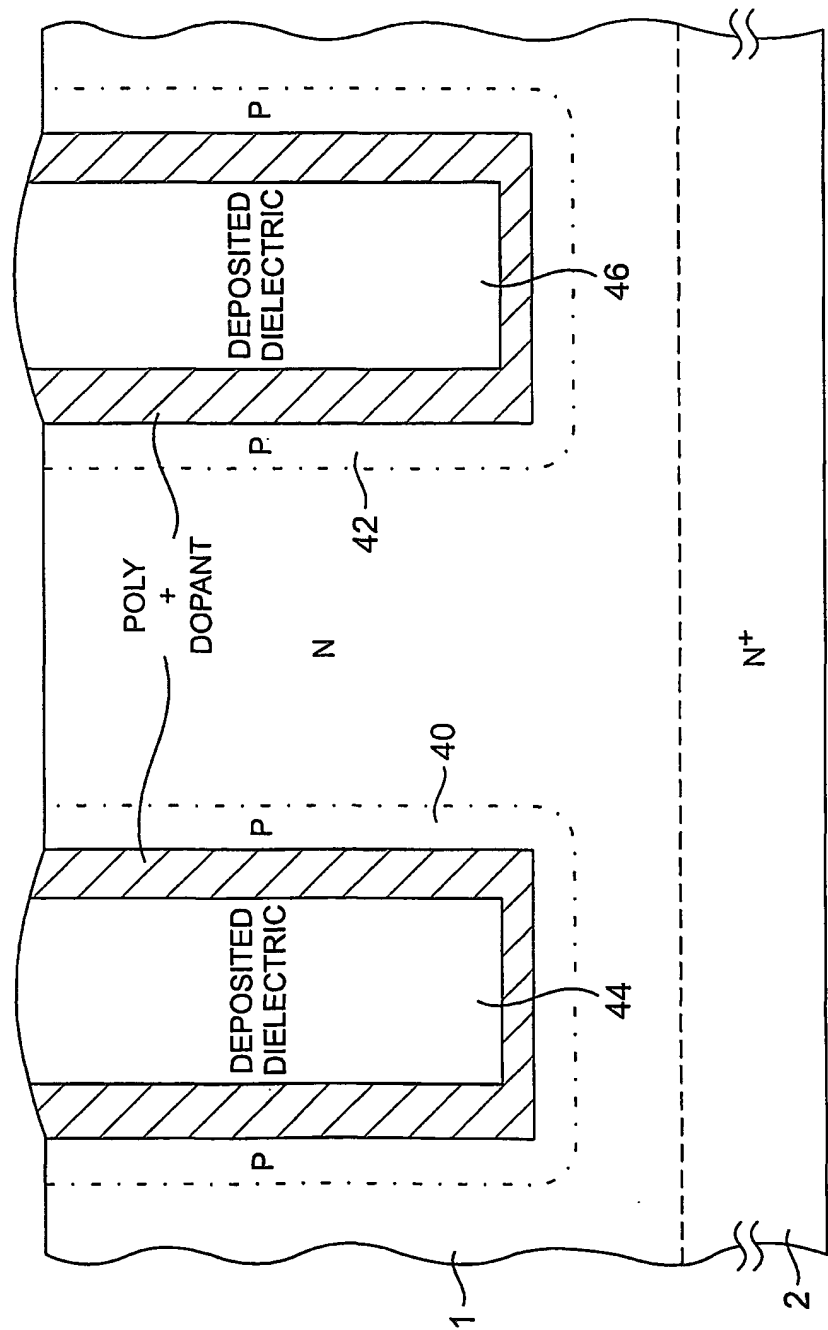
A DOPING PROFILE THAT WAS DIFFUSED FROM TRENCHES FILLED WITH DOPANT-RICH DIELECTRIC

FIG. 4



A DOPING PROFILE THAT WAS DIFFUSED FROM
TRENCHES CONTAINING DOPED POLYCRYSTALLINE
SILICON THAT WAS SUBSEQUENTLY OXIDIZED

FIG. 5



A DOPING PROFILE THAT WAS DIFFUSED FROM A TRENCH CONTAINING DOPED POLYCRYSTALLINE SILICON AS WELL AS DEPOSITED DIELECTRIC

FIG. 6

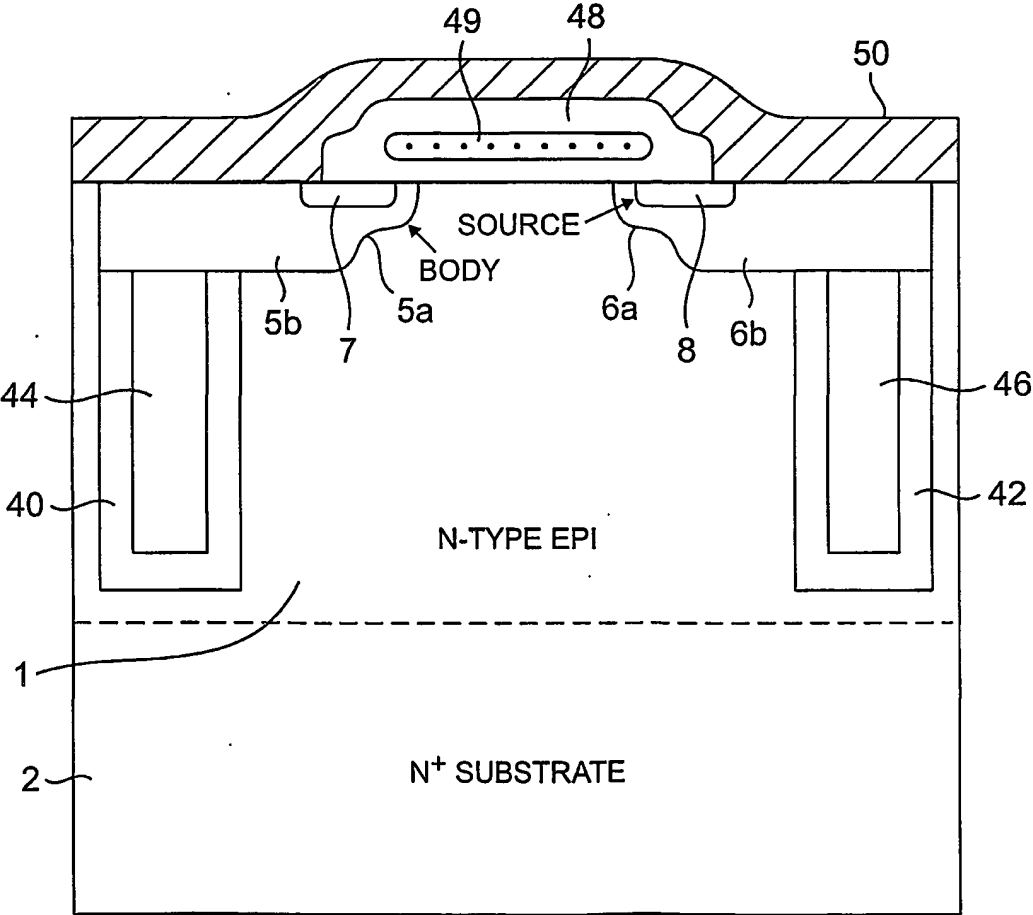


FIG. 7

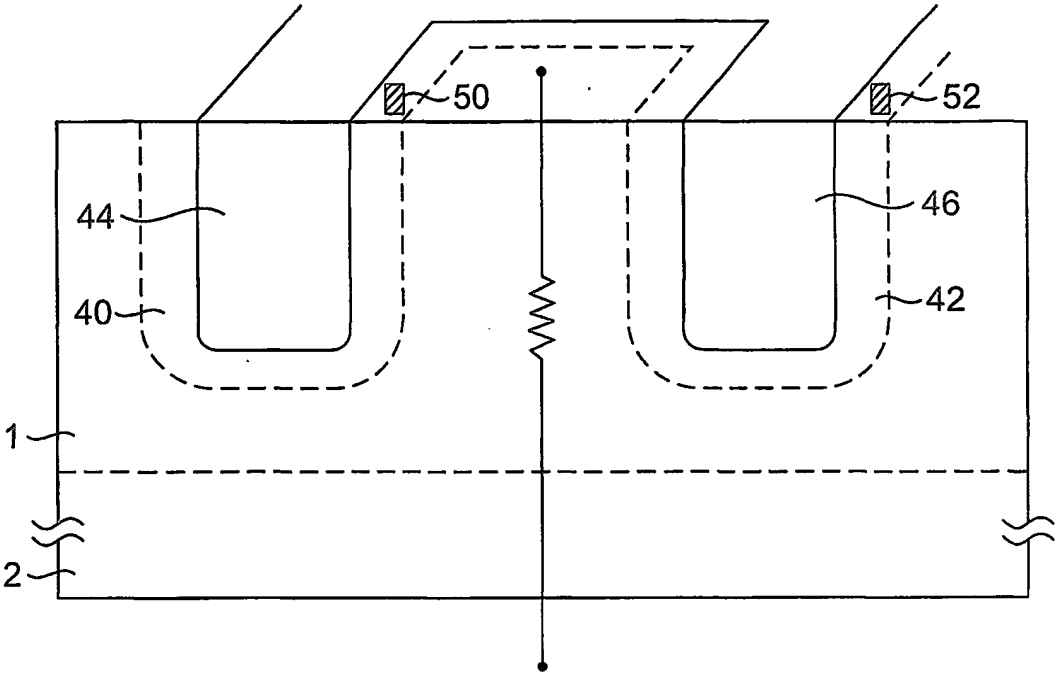


FIG. 8A

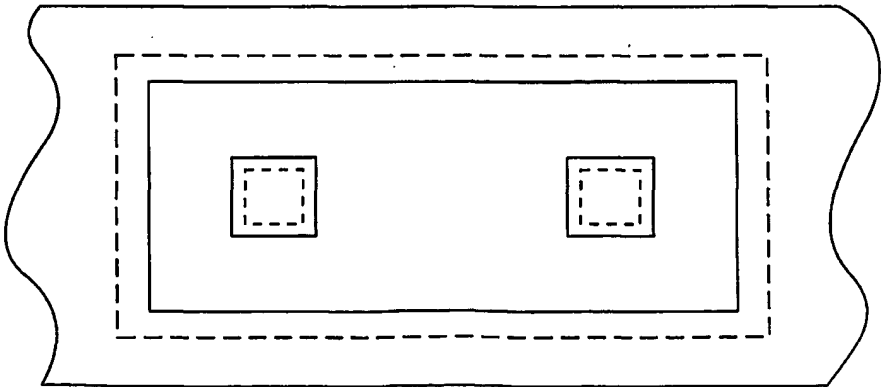
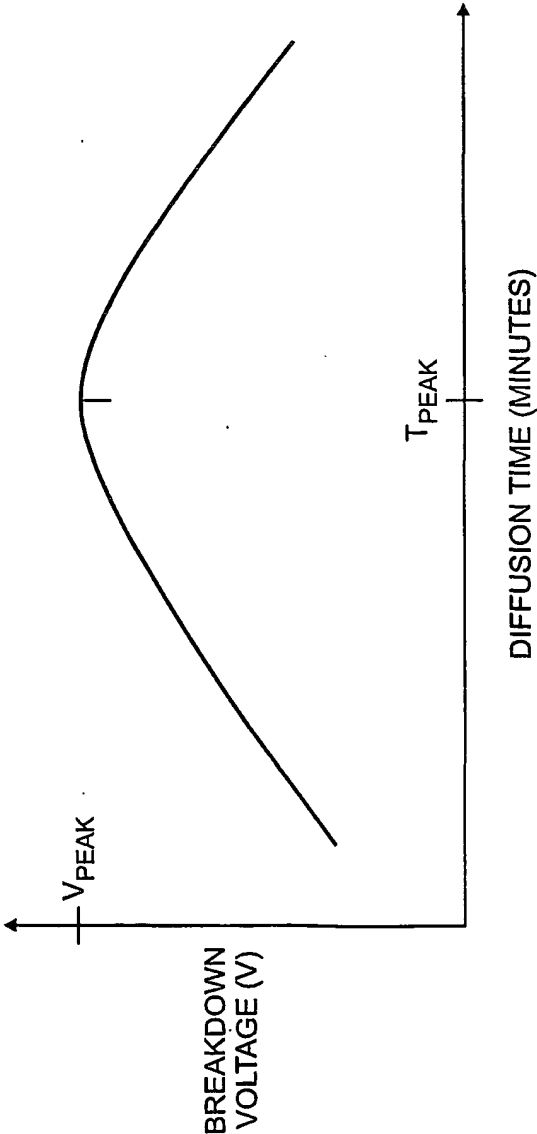
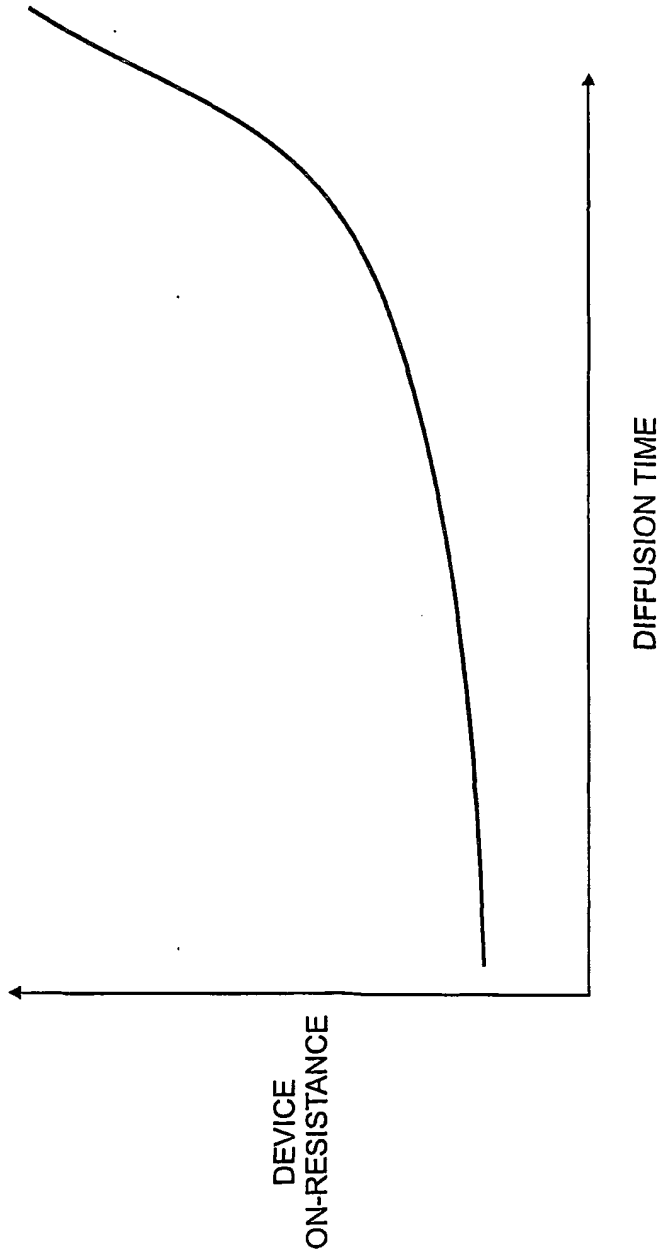


FIG. 8B



THE RELATIONSHIP BETWEEN DIFFUSION TIME AND
BREAKDOWN VOLTAGE OF THE STRUCTURE OF FIG. 5

FIG. 9



THE RELATIONSHIP BETWEEN DEVICE
ON-RESISTANCE AND DIFFUSION TIME

FIG. 10

INTERNATIONAL SEARCH REPORT

Int. and Application No.

PC 1/JS 01/18007

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L21/336 H01L21/66 H01L21/225 H01L29/78 H01L29/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 02, 28 February 1997 (1997-02-28) -& JP 08 264772 A (TOYOTA MOTOR CORP), 11 October 1996 (1996-10-11)	12
A	abstract; paragraphs '0030!-'0039!; figures 5,8,9 --- -/--	1,2,5, 10,11



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *8* document member of the same patent family

Date of the actual completion of the international search

19 October 2001

Date of mailing of the international search report

29/10/2001

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 opo nl,
Fax: (+31-70) 340-3016

Authorized officer

Morvan, D

INTERNATIONAL SEARCH REPORT

International Application No.

PC 1/JS 01/18007

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GLENN J ET AL: "A novel vertical deep trench RESURF DMOS (VTR-DMOS)" PROCEEDINGS OF THE 12TH INTERNATIONAL SYMPOSIUM ON POWER SEMICONDUCTOR DEVICES & ICS, TOULOUSE, FR, 22 - 25 May 2000, pages 197-200, XP000974099 IEEE, Piscataway, NJ, USA ISBN: 0-7803-6269-1	12
A	paragraph II; figure 1	1,2,5,6, 10,11
X	--- US 5 216 275 A (CHEN X) 1 June 1993 (1993-06-01)	12
A	column 5, line 30 -column 6, line 2; figures 2-5	1,2,10
A	--- DE 197 48 523 A (SIEMENS AG) 12 May 1999 (1999-05-12) column 3, line 65 -column 4, line 11; figures 2,6 -----	1,3,4, 10,12

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 01/18007

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
JP 08264772	A	11-10-1996	NONE	
US 5216275	A	01-06-1993	CN 1056018 A	06-11-1991
DE 19748523	A	12-05-1999	DE 19748523 A1	12-05-1999
			WO 9923704 A1	14-05-1999
			EP 1029362 A1	23-08-2000